TGA2567-SM

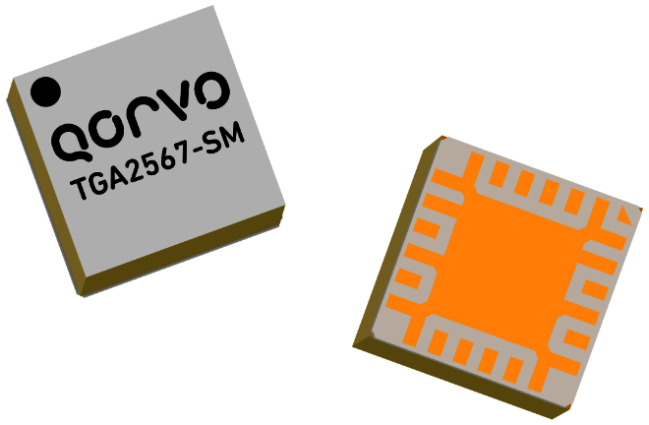
2 – 20 GHz LNA Amplifier

Product Description

Qorvo's TGA2567-SM is a LNA Gain Block fabricated on Qorvo's proven 0.15um pHEMT production process.

The TGA2567-SM operates from 2 to 20 GHz and typically provides 19 dBm of 1dB compressed output power with 17 dB of small signal gain. Greater than 16 dB of adjustable gain can be achieved by varying V_{G2}. The Noise Figure is typically 2 dB at mid band.

The TGA2567-SM is available in a low-cost, surface mount 24 lead 4x4 AIN QFN package base with an Air cavity laminate lid. TGA2567-SM is ideally suited to support both commercial and defense related applications.

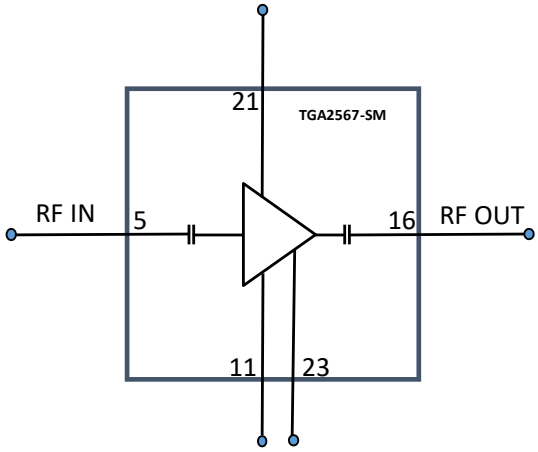


QFN 4x4 mm 24L

Product Features

- Frequency Range: 2 – 20 GHz
- P_{SAT}: 22 dBm
- P_{1dB}: 19 dBm
- Small Signal Gain: 17 dB
- Adjustable Gain Range (using V_{G2})
- Noise Figure: 2 dB
- OIP3: 29 dBm
- Bias: V_D = 5 V, I_D = 100 mA, V_{G1} = -0.7 V typical, V_{G2} = +1.3 V
- ESD Protection Circuitry on V_D, V_{G1} and V_{G2}
- Package dimensions: 4.00 x 4.00 x 1.625 mm

Functional Block Diagram



Applications

- General Purpose LNA/Gain Block
- Point to Point Radio
- Electronic Warfare
- Military & Commercial Radar
- Communications

Ordering Information

Part No.	Description
TGA2567-SM	2 – 20 GHz LNA / Gain Block
TGA2567-SMEVB	TGA2567-SM Evaluation Board, Qty 1

Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
Drain Voltage (V_D)	-	6	V
Drain to Gate Voltage (V_D-V_{G1})	-	8	V
Gate Voltage Range (V_{G1})	−2	1	V
Gate Voltage Range (V_{G2})	−2	4	V
Drain Current (I_D)	-	160	mA
Gate Current Range (I_{G1}, I_{G2})	-1	40	mA
Power Dissipation (P_{DISS})	-	2.8	W
RF Input Power, CW, 50 Ω, T =25 °C	-	22	dBm
Channel Temperature (T_{CH})	-	200	°C
Mounting Temperature (30 Seconds)	-	260	°C
Storage Temperature	−55	150	°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Value / Range	Units
Drain Voltage (V_D)	5	V
Drain Current (I_{DQ})	100	mA
Gate Voltage (V_{G1}), typical, can be adjusted to get I_{DQ}	-0.7	V
Gate Voltage (V_{G2}), can be adjusted for gain control	+1.3	V
Operating Temperature Range (T_{BASE})	−40 to 85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	2	–	20	GHz
Small Signal Gain	–	17	–	dB
Input Return Loss	–	15	–	dB
Output Return Loss	–	14	–	dB
Noise Figure: 2 GHz	–	2.8	–	dB
Output TOI	–	29	–	dBm
Output Power (Saturation; P_{IN} = 10 dBm)	–	22	–	dBm
Output Power (1 dB Compression)	–	19	–	dBm
Small Signal Gain Temperature Coefficient	–	-0.013	–	dB/°C
Noise Figure Temperature Coefficient	–	0.009	–	dB/°C

Test conditions unless otherwise noted: 25 °C, V_D = +5 V, I_{DQ} = 100 mA, V_{G1} = −0.7 V Typical, V_{G2} = 1.3 V
Data are de-embedded to package.

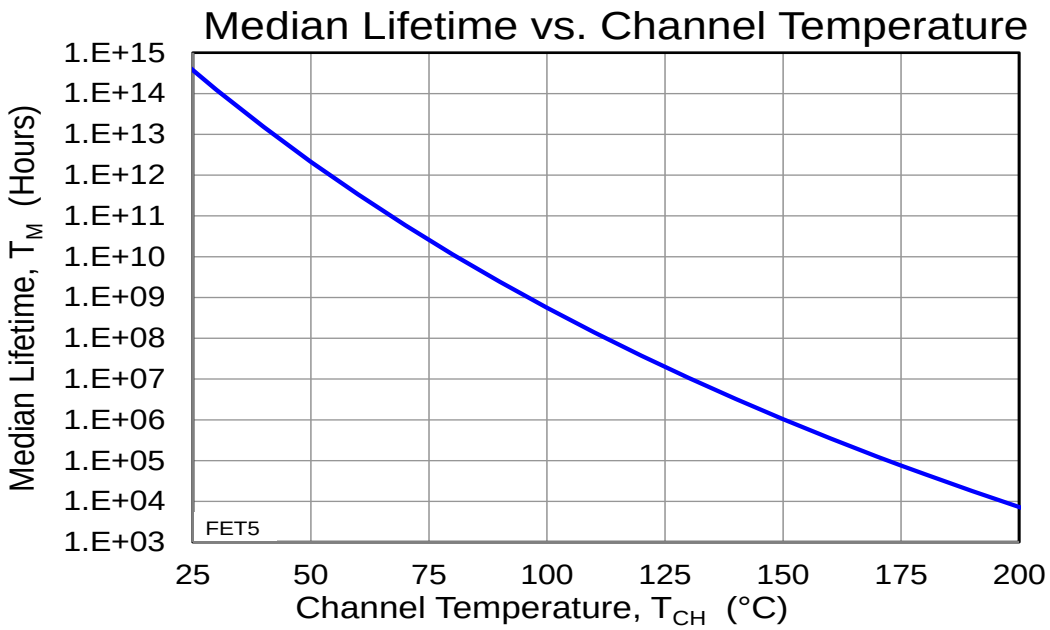
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Tbaseplate = 85 °C	41	ºC/W
Channel Temperature, T_{CH} (Without RF Drive)	Tbaseplate = 85 °C, V_D = 5 V, I_{DQ} = 100 mA, P_{DISS} = 0.5 W	106	°C
Median Lifetime, T_M (Without RF Drive)		2.4 x 10^8	Hrs
Channel Temperature, T_{CH} (Under RF Drive)	Tbaseplate = 85 °C, V_D = 5 V, I_{DD} = 156 mA, P_{OUT} = 22.8 dBm, P_{DISS} = 0.59 W	109	°C
Median Lifetime, T_M (Under RF Drive)		1.6 x 10^8	Hrs

Notes: (1) Thermal resistance measured to back of package.

Median Lifetime

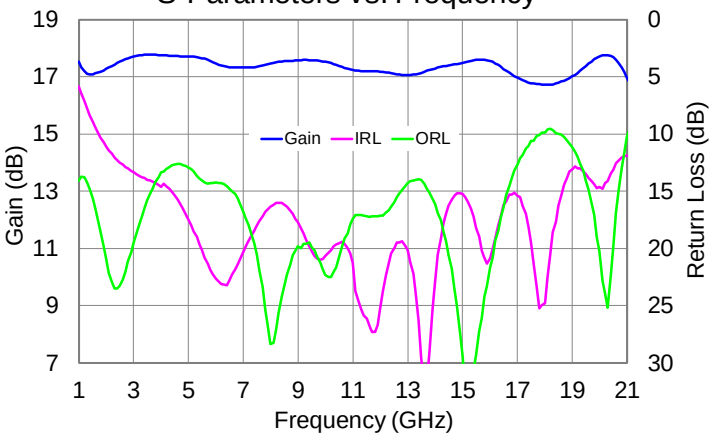
Test Conditions: V_D = 6 V; Failure Criteria = 10 % reduction in ID_MAX during DC Testing



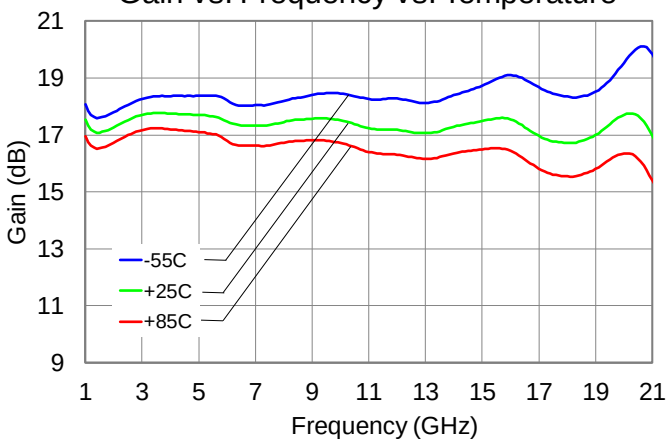
Performance Plots – Small Signal & Noise Figure

Conditions unless otherwise specified: V_D = 5 V, I_{DQ} = 100 mA, V_{G1} = -0.7 V Typical, V_{G2} = 1.3 V, 25 °C

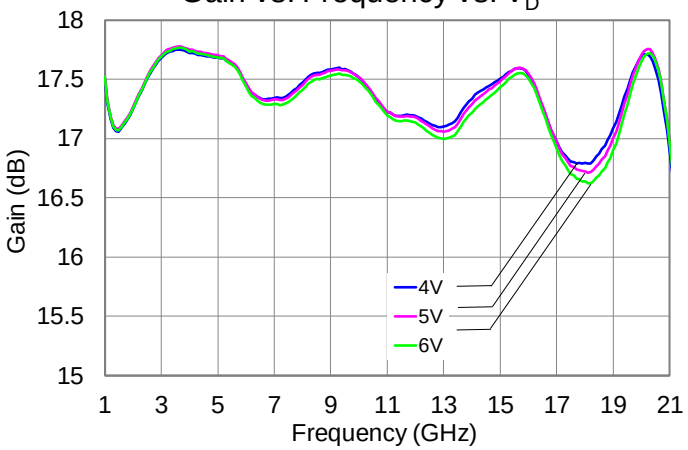
S-Parameters vs. Frequency



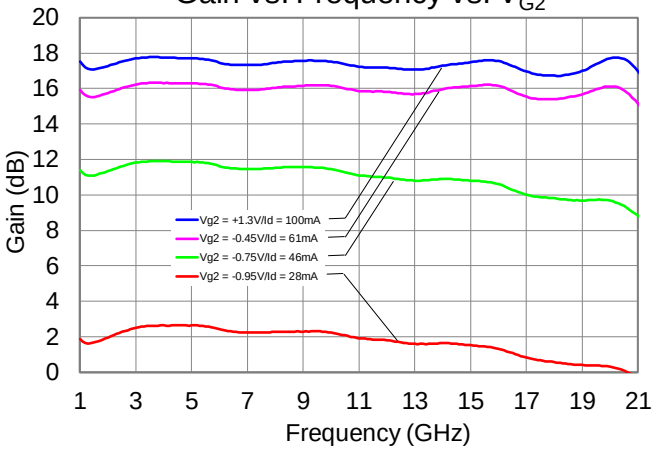
Gain vs. Frequency vs. Temperature



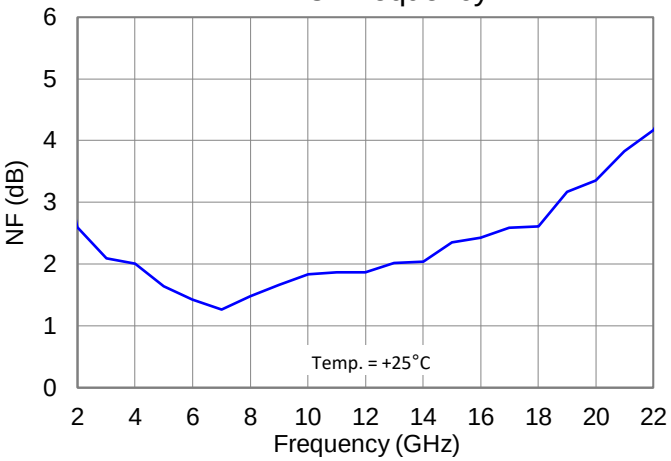
Gain vs. Frequency vs. V_D



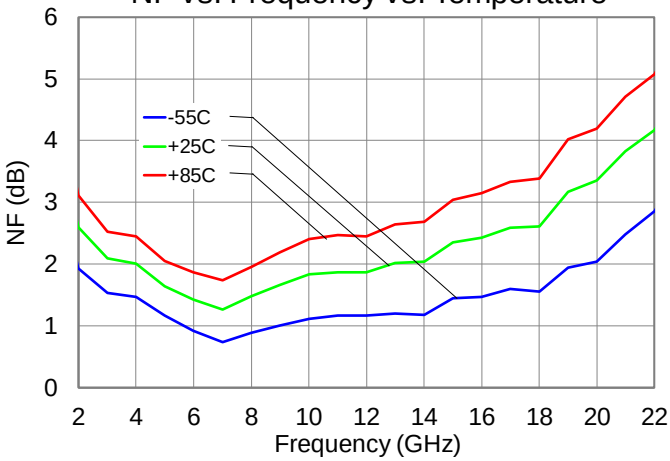
Gain vs. Frequency vs. V_{G2}



NF vs. Frequency

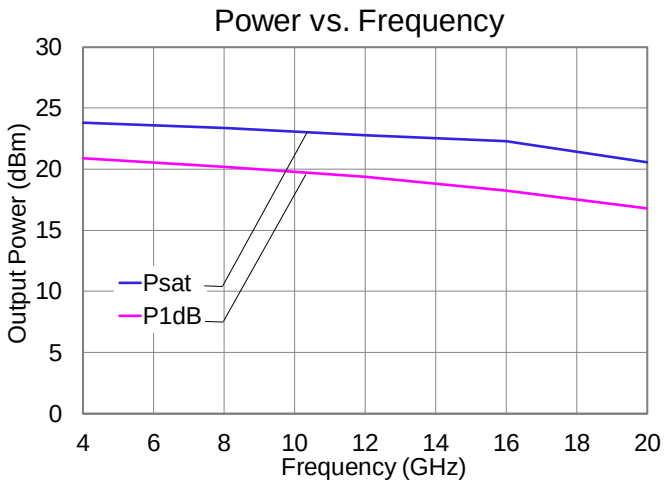


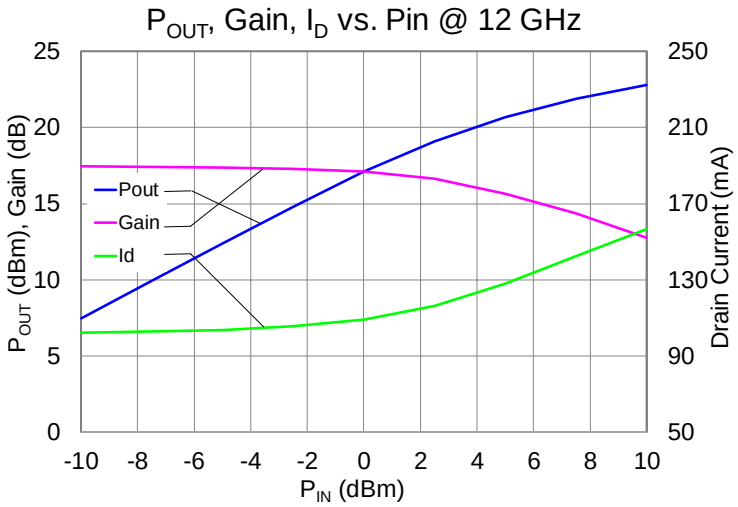
NF vs. Frequency vs. Temperature

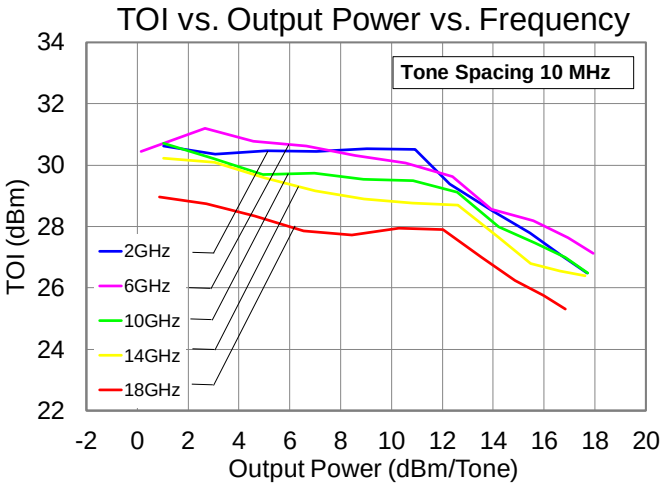


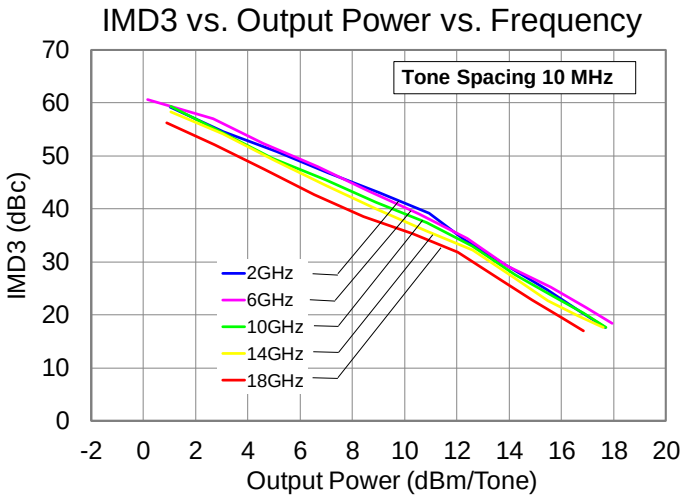
Performance Plots – Large Signal & Linearity

Conditions unless otherwise specified: V_D = 5 V, I_{DQ} = 100 mA, V_{G1} = -0.7 V Typical, V_{G2} = 1.3 V. 25 °C

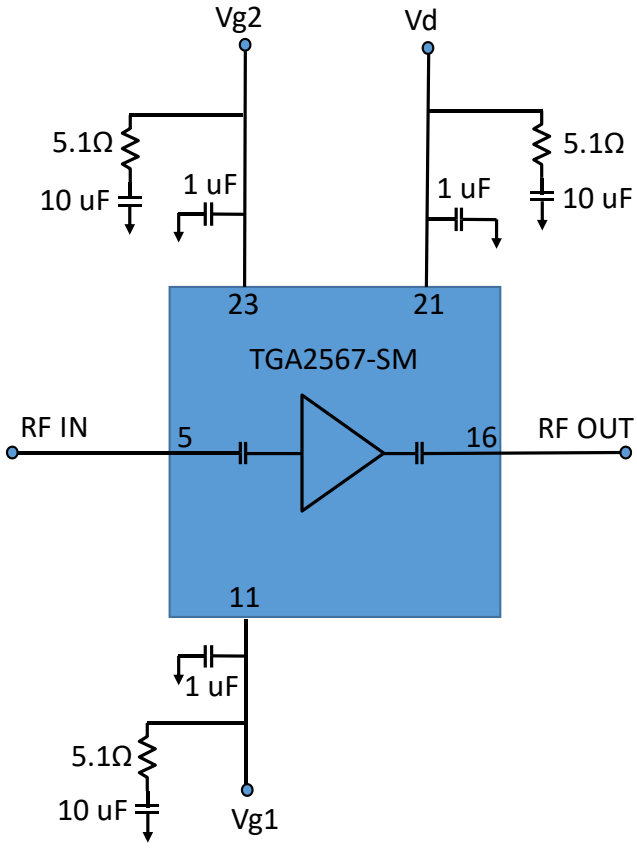








Applications Information



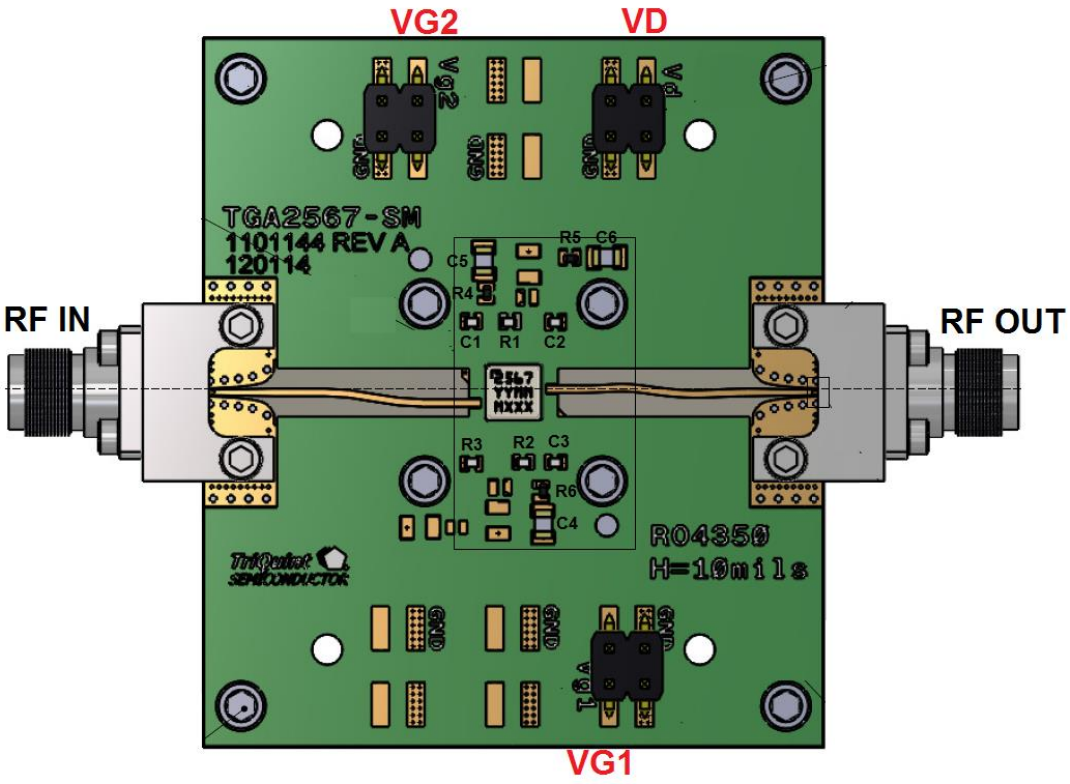
Bias Up Procedure

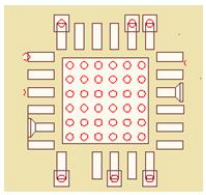
1. Set I_D limit to 160 mA, I_G limit to 24 mA
2. Apply −1.5 V to V_{G1}
3. Apply +5 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Apply +1.3 V to V_{G2}
5. Adjust V_{G1} until I_{DQ} = 100 mA (V_{G1} ~ −0.7 V Typ.)
6. Adjust V_{G2} to obtain desired gain
7. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_{G1} to −1.5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_{G2} to 0 V
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G1} and V_{G2} supplies

Evaluation Board Layout Assembly and Mounting Pattern





Mounting Detail

Top dielectric material is ROGERS 4350, 0.010 inch thickness with 0.5 oz copper.

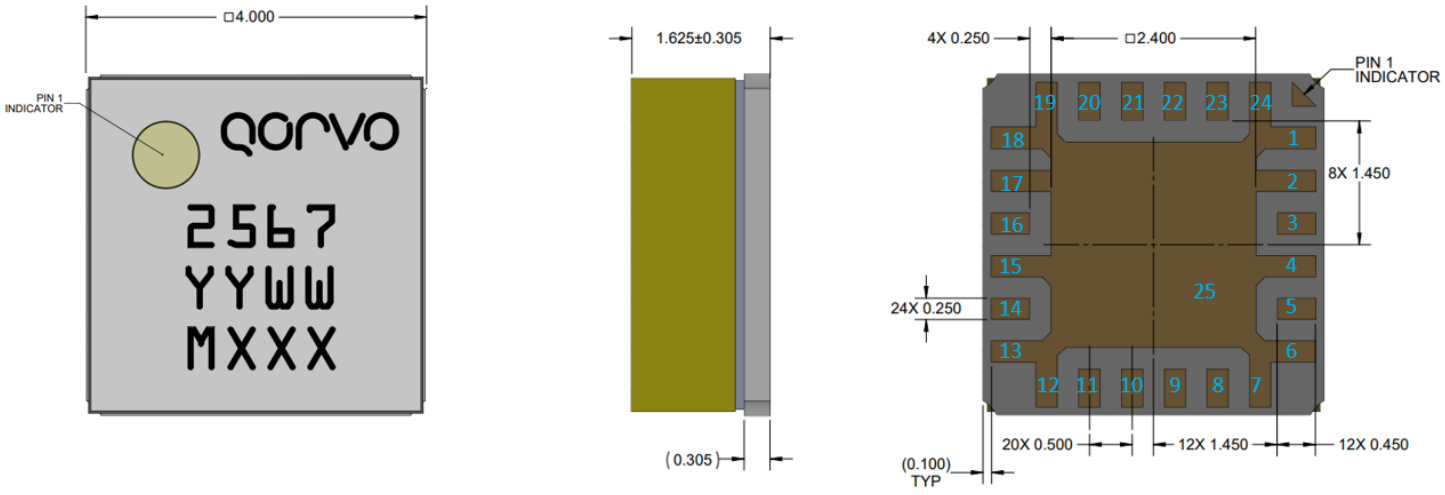
The pad pattern shown above has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008 in. diameter drill, filled with copper plating.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2, C3	1.0 µF	Cap, 0402, +16V, ±20 %, X5R	Various	–
C4, C5, C6	10.0 µF	Cap, 0805, +10 V, ±10 %, X7R	Various	–
R4, R5, R6	5.1 Ω	Res, 0402, SMT	Various	–

Mechanical Drawing



All dimensions are in millimeters.

Marking: Part number – 2567, Year/Month code – YYMM, Batch ID – MXXX.
Package is air-cavity. Materials: Ceramic with laminate lid.
Part is epoxy sealed, finish pads are gold plated.

Pad Description

Pin	Symbol	Description
1,2,4,6,7,12,13,15,17-19,24	GND	Backside paddles; must be grounded on PCB. Multiple vias should be employed to minimize inductance and thermal resistance. (2)
3,8-10,14,20,22	N/C	No internal connection; must be grounded on PCB.
5	RF IN	RF input
11	V_{G1}	Gate voltage. Bias network is required.
16	RF OUT	RF output.
21	V_D	Drain voltage. Bias network is required.
23	V_{G2}	Gate voltage. Bias network is required.
25	GND	Back side ground base

Solderability

1. Compatible with lead-free soldering process with 260° C peak reflow temperature.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile